Evidence for suppressed short-channel effects in deep submicron dual-material gate (DMG) partially depleted SOI MOSFETs - A two-dimensional analytical approach

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Abstract

Short-channel effects in a dual-material gate partially depleted (DMG-PD) silicon-on-insulator (SOI) MOSFET are studied by developing a 2-D analytical model for the surface potential variation along the channel. The model includes the calculation of the surface potential, electric field along the channel and threshold voltage using the minimum surface potential. The model takes into account the effects of body doping concentration, gate oxide, buried oxide and silicon film thickness, lengths of the gate metals and their work functions, applied drain and substrate biases. It is seen that short channel effects in this structure are suppressed because of the perceivable step in the surface potential profile, which screens the drain potential. It is also seen that the model predicts a threshold voltage roll-up as the channel length is reduced. The results predicted by the model are compared with those obtained by two-dimensional simulation to verify the accuracy of the proposed analytical model.

Keywords: Dual material gate; Partially depleted; Silicon-on-insulator MOSFET; Surface potential; Threshold voltage; Two-dimensional modeling

1. Introduction

Thin film SOI MOSFETs offer a number of advantages viz. low power dissipation, higher operating speed, denser packing, elimination of latch-up, simpler design, radiation-hardness and improved immunity to short channel effects[1-3]. They can be either fully depleted (FD) or partially depleted (PD). The focus of this paper is on partially depleted SOI MOSFETs.

With the continuous down scaling of the CMOS technology into the deep-submicron era,
the control of the gate on the threshold voltage decreases as the channel length shrinks because of the increased charge sharing from source and drain. Therefore the threshold voltage reduction with decreasing channel lengths and drain induced barrier lowering are the issues that need to be addressed while providing immunity against short-channel effects (SCEs) [1]. There are several techniques to control the SCEs in SOI MOSFETs such as the graded channel engineering.

As discussed in a review on SOI MOSFETs[1], to enhance the immunity against short channel effects, a number of solutions have been proposed in literature such as (i) thin body SOI with raised source and rain, (ii) buried insulator engineering, (iii) graded channel SOI, (iv) halo doped SOI, (v) ground plane SOI, and (vi) multiple gate SOI. Recently, an interesting structure known as the dual material gate in a bulk MOSFET was proposed [4], [5] to contain the short-channel effects. It has been shown that in the DMG MOSFET, there is a simultaneous increase in transconductance and suppressed short channel effects due to a step in the surface potential profile. In this structure, the peak electric field at the drain end is reduced, which ensures that the average electric field under the gate is increased. This enables an increased lifetime of the device, minimization of the ability of the localized charges to raise drain resistance and more control of gate over the conductance of the channel so as to increase the gate transport efficiency. Due to different work functions, the surface potential profile is a step function, which ensures reduction in the short-channel effects and screening of the channel region under M1 from drain potential variations. After saturation, M2 absorbs any additional drain-source voltage and hence the region under M1 is screened from the drain potential variations[4]. The primary objective here is to apply the dual gate concept to a partially depleted SOI MOSFET and explain the unique features offered by this structure. An analytical model using Poisson’s equation also has been presented for the surface potential and threshold model for the DMG-PD SOI MOSFET. The model results are verified by comparing with the results obtained from two-dimensional simulation [6]. A very close match has been found between the model and simulation results.

2. Mathematical model for surface potential

Fig. 1 shows the cross section of the DMG-PD SOI MOSFET with metal gates M1 and M2 of lengths $L_1$ and $L_2$, respectively. The work functions of metal gates M1 and M2 are $\Phi_M^1 = 4.63$ eV and $\Phi_M^2 = 4.17$ eV, respectively. The channel length $L$ in the DMG structure is the sum of lengths $L_1$ and $L_2$ and in the case of SMG, the channel length is same as the above L but with a gate having a uniform workfunction of $\Phi_M = 4.63$ eV. In the PD SOI MOSFET structure the film thickness can be divided into four regions—two of them being the depleted regions on the source and drain side, respectively, and the other two being the partially depleted regions below the metal gates. For simplicity, in the model derivation, we have taken into account only the partially depleted regions below the metal gates. The fully depleted regions on source and drain have been neglected for the body doping concentration chosen in our structure ($1 \times 10^{18}$ cm$^{-3}$).

Assuming that the impurity density in the channel region is uniform and neglecting the influence of charge carriers on the electrostatics of the channel, the potential distribution in the silicon thin-
film, before the onset of strong inversion can be written as

\[
\frac{d^2\phi}{dx^2} + \frac{p}{\varepsilon_{ij}} \frac{d^2\phi}{dy^2} = \frac{qN_A}{\varepsilon_{ij}}
\]

for \(0 \leq x \leq L\), \(0 \leq y \leq w_d\),

where \(N_A\) is the body doping concentration, \(\varepsilon_{si}\) is the silicon dielectric constant, \(L\) is the device channel length, \(w_d\) is the channel depletion width and is given by

\[
w_d = \sqrt{\frac{2\varepsilon_{si}\delta 2(V_B + V)}{qN_A}}.
\]

The potential profile in the vertical direction is assumed to be a second order polynomial [7], i.e.,

\[
\phi(x,y) = \phi_s(x) + a_1 y + a_2 y^2,
\]

where \(\phi_s(x)\) is the surface potential and \(a_1\) and \(a_2\) are arbitrary constants which are functions of \(x\) only. In the DMG structure we have two different materials with different work functions \(\phi_{M1}\) and \(\phi_{M2}\). Therefore the flat-band voltages of the two gates would be different and they are given as

\[
\phi_{FB1} = \phi_{M1} - \phi_s \quad \text{and} \quad \phi_{FB2} = \phi_{M2} - \phi_s,
\]

where \(\phi_s\) is the semiconductor work function which is given by

\[
\phi_s = \frac{E_g}{2q} + \phi_F,
\]

where \(E_g\) is the silicon bandgap, \(\phi_F\) is the electron affinity. Since we have two regions in the DMG structure, the potential under the metal gates M1 and M2 can be written as

\[
\phi_1(x,y) = \phi_{si}(x) + a_11 \delta x p y + a_21 \delta x y^2
\]

for \(0 \leq x \leq L_1\),

\[
\phi_2(x,y) = \phi_{si}(x) + a_12 \delta x p y + a_22 \delta x y^2
\]

for \(L_1 \leq x \leq L_1 + \delta L_2\), \(0 \leq y \leq w_d\).

The Poisson’s equation is solved separately under the two gate regions using the following boundary conditions.

1. Surface potential at the interface of the two dissimilar metals is continuous

\[
\phi_1(L_1,0) = \phi_2(L_1,0) = \phi_{L1},
\]

where \(\phi_{L1}\) is the surface potential at \(x = L1\).

2. Potential at the depletion edge is given by

\[
\phi_i(x,w_d) = (j)_i(x,w_d) = (j)_B
\]

where \(j_B\) is the body electrostatic potential.

3. Electric flux at the interface of the two dissimilar metals is continuous

\[
\frac{d\phi_i}{dx} \bigg|_{x=L_1} = \frac{d\phi_j}{dx} \bigg|_{x=L_2},
\]

4. Electric field at the interface of gate/oxide is continuous for both the metal gates

\[
\frac{d\phi_i}{dx} \bigg|_{y=0} = \frac{\epsilon_{ox}}{\epsilon_{si}} \frac{\phi_{i1}(x) - V_{GS1}'}{t_{ox}},
\]

\[
\frac{d\phi_j}{dx} \bigg|_{y=0} = \frac{\epsilon_{ox}}{\epsilon_{si}} \frac{\phi_{j2}(x) - V_{GS2}'}{t_{ox}},
\]

where \(\epsilon_{ox}\) is the dielectric constant of the oxide, \(t_{ox}\) is the gate oxide thickness and

\[
V_{GS1}' = V_{GS} - V_{FB1} \quad \text{and} \quad V_{GS2}' = V_{GS} - V_{FB2},
\]

where \(V_{GS}\) is the gate-to-source bias voltage, \(V_{FB1}\) and \(V_{FB2}\) are the front-channel flat-band voltages of metal 1 and metal 2, respectively.

5. Electric field at the depletion edge is zero, i.e.,

\[
\frac{d\phi_i}{dx} \bigg|_{y=w_d} = \frac{d\phi_j}{dx} \bigg|_{y=w_d} = 0
\]

6. Potential at the source end is

\[
\phi_i(O,0) = 0, \phi_j(O,0) = K_{br},
\]

7. Potential at the drain end is

\[
\phi_1(L,0) = \phi_2(L) = V_{bi} + V_{DS},
\]

where \(L = L1 + L2\). VDS is the applied drain-source bias and \(Fy\) is the built in potential given by
\[ V_u = V_T N \left( \frac{N_A N_D}{n_i^2} \right) \]

where \( N_D \) is the source/drain doping concentration.

The expression for the constants \( a_1(x), a_2(x), a_1(x), a_2(x) \) can be found from the boundary conditions (11), (12) and (14). Substituting their values in (6) and (7) and then in (1) we get

\[ \frac{d^2 \phi_1(x)}{dx^2} + \phi_1(x) \phi_0 = c_1 \phi_0 \]

\[ \frac{d^2 \phi_2(x)}{dx^2} + \phi_2(x) \phi_0 = \gamma_2 \phi_0 \]

where

\[ a = \gamma \left( \frac{3}{w_d} \frac{2}{w_d} + \frac{6 \varepsilon_{ox} \varepsilon_{flu}}{\varepsilon_{flu} \varepsilon_{ox} w_d} \right) \]

\[ \beta = \frac{12 \gamma y}{w_d} \frac{6 \varepsilon_{ox} \varepsilon_{flu}}{\varepsilon_{flu} \varepsilon_{ox} w_d} - \frac{4 \varepsilon_{ox}}{\varepsilon_{flu} \varepsilon_{ox} w_d} \]

The above equations are second order differential equations and the expression for surface potential under both the metal gates is of the form

\[ \phi_s(x) = A_1 \exp(\eta L) + B_1 \exp(-\eta L) \]

\[ \phi_s(x) = A_2 \exp(\eta L) + B_2 \exp(-\eta L) \]

where \( g = \sqrt{\frac{T}{T}} \). The expressions for \( A_1, B_1, A_2 \) and \( B_2 \) can deduced with the help of (8), (15) and (16) and are given by

\[ A_1 = \frac{- (V_m - \sigma_1) + (\phi_{L1} - \sigma_1) \exp(\eta L_1)}{\exp(2\eta L_1) - 1} \]

\[ B_1 = \frac{(V_b \exp(2\eta L_1) - \phi_{L1} \exp(\eta L_1))}{\exp(2\eta L_1) - 1} \]

\[ A_2 = \frac{(V_b + V_D - \sigma_2) \exp(\eta L) + (\phi_{L1} - \sigma_2) \exp(\eta L_1)}{\exp(2\eta L) - \exp(2\eta L_1)} \]

where \( r_1 = c_1 / b \) and \( r_2 = c_2 / b \). Since the electrostatic potential and the electric field are continuous at the interface of the region below the two gates as indicated by the boundary condition 1 in (8), the value of \( \phi L \) can be obtained using (10) as:

\[ \phi L = \left\{ \frac{2(V_b + V_D - \phi L) \exp(\eta L_1) + \phi_{L1} \exp(2\eta L_1) + \phi_{L2} \exp(2\eta L)}{\exp(2\eta L_1) - 1} \right\} \]

\[ \phi L = \left\{ \frac{2(V_b + V_D - \phi L) \exp(\eta L_1) + \phi_{L1} \exp(2\eta L_1) + \phi_{L2} \exp(2\eta L)}{\exp(2\eta L_1) - 1} \right\} \]

In the case of DMG structure, due to the co-existence of metal gates, M1 and M2 with different work functions, the surface potential minima is solely determined by the metal gate with higher work function. For NMOSFET (present case) the work function of M1 is greater than that of M2 and for
PMOSFET it is vice-versa. The minima of the surface potential \( \psi_{s1,\text{min}} \), occurs at

\[
V_{\text{th}} = V_{FB1} - \left( \frac{2/\beta - KL \exp(\gamma/x_{\text{min}}) - K_2 \exp(-\gamma/x_{\text{min}})}{1 + K_3 \exp(\gamma/x_{\text{min}}) + K_4 \exp(-\gamma/x_{\text{min}})} \right) - \frac{qN_A}{e_{\text{si}}} \left( \frac{s_{oix} \omega_{d}}{4\varepsilon_{\text{ox}}} \right)^{1/2} \]

The minimum surface potential can be obtained by substituting for \( x = x_{\text{min}} \) in (19) which is given as

\[ \psi_{s,\text{mm}} = A^i \exp(\gamma/x_{\text{mm}}) + B^i \exp(-\gamma/x_{\text{mm}}) + j. \]

An expression for the electric field can be obtained by differentiating the surface potential expressions (19) and (20) and is given by

\[
E_1(x) = \frac{d\psi_1(x,y)}{dx} \bigg|_{y=0} \approx A_1 \eta \exp(\eta x) - B_1 \eta \exp(-\eta x) \quad 0 \leq x \leq L_1
\]

\[
E_2(x) = \frac{d\psi_2(x,y)}{dx} \bigg|_{y=0} = A^i \exp(\gamma/x) - B^i \exp(-\gamma/x) \quad L_1 \leq x \leq L.
\]

The above two equations are quite useful in determining how the drain side electric field is modified by the DMG structure.

### 3. Threshold voltage model

The threshold voltage \( V_{\text{th}} \) is that value of the gate voltage \( V_{GS} \) at which a conducting channel is induced at the surface of SOI MOSFET. Therefore, the threshold voltage is taken to be that value of gate source voltage for which \( \psi_{s1,\text{min}} - 2\psi_F \) where \( \psi_F \) is the difference between the extrinsic Fermi level in the bulk region and the intrinsic Fermi level. Hence we can determine the value of threshold voltage as the value of \( V_{GS} \) by solving the expression for \( \psi_{s1,\text{min}} \) as given below:

\[ K_1 = \frac{-V_{FB1} + \psi_F \exp(\eta L_1)}{\exp(2\eta L_1) - 1} \]

\[ K_2 = \frac{\psi_F \eta \exp(\eta L_1) - 4\psi_F \eta \exp(\eta L_1)}{\exp(2\eta L_1) - 1} \]

\[ K_3 = \frac{1 - \exp(\eta L_1)}{\beta \exp(2\eta L_1) - 1} \]

\[ K_4 = \frac{-\exp(2\eta L_1) + \exp(\eta L_1)}{\beta \exp(2\eta L_1) - 1} \]

The dependence of the surface potential on the work functions of the metal gates means that we can tune the surface potential and the threshold voltage of the transistor. This mechanism has also been observed for bulk MOSFETs [8] and fully de-

![Surface channel potential profiles](image-url)

**Fig. 2.** Surface channel potential profiles of a partially depleted DMG-SOI MOSFET obtained from the analytical model and MEDICI simulation for different drain biases with a channel length \( L = 0.15 \) \( \mu \text{m} \) (\( L_1 = 0.05 \) \( \mu \text{m} \) and \( L_2 = 0.1 \) \( \mu \text{m} \)). The parameters used are: \( t_{ox} = 2 \) nm, \( t_b = 450 \) nm, \( 4; = 100 \) nm and \( \phi_b = 0 \) V.
pleted SOI MOSFETs [9] when dual material gate concept is applied.

4. Results and discussion

2-D device simulator MEDICI [6] is used to verify the results of the proposed model. Fig. 2 shows the calculated and simulated values of the surface potential for $L = 0.15 \ \mu m$ for different drain voltages along the channel for a channel length of 0.15 $\mu m$. The predicted values of the model agree well with the simulation results. It is clearly seen that because of the step function profile of the surface potential, there is no significant increase of the potential under gate M1 as the drain voltage is increased, which means that gate M1 is effectively screened from the drain potential variations. In other words, the drain voltage has very little influence on the drain current after saturation, thus reducing the drain conductance. It follows from the figure that the minimum surface potential point is independent of the applied drain bias.

Fig. 3 shows the calculated and simulated values of electric field along the channel length at the drain end for the DMG-PD SOI MOSFET and the simulated values for SMG-PD SOI MOSFET for the same channel length. It clearly shows that there is a considerable reduction in the peak electric field at the drain end in the case of the DMG structure when compared with SMG. This reduction in the electric field reduces the hot carrier effect, which is another important short channel effect. The agreement between the model and simulated results proves the accuracy of the model.

Fig. 4. Variation of the channel minimum potential with channel length $L = L_1 + L_2$ for partially depleted DMG-SOI MOSFET's with $L_1$ constant at 0.05 $\mu m$. The parameters used are: $V_{DS} = 50 \ \text{mV}$, $V_{GS} = 0.15 \ \text{V}$, $t_{ox} = 5 \ \text{nm}$, $t_b = 450 \ \text{nm}$, $/g = 0 \ \text{V}$ and $N_A = 1 \times 10^{18} \ \text{cm}^{-3}$.
Minimum surface potential as a function of channel length $L (=L_1 + L_2)$ for partially depleted DMG-SOI with film thickness $t_{si} = 100$ nm is shown Fig. 4. As previously stated, Fig. 4 points out that the minimum channel potential is almost constant for different channel lengths. This is due to the existence of a work function difference in the case of DMG-SOI MOSFET’s. The close match between the analytical results and the 2-D simulation results verifies the validity of model for the minimum surface potential under the gate for different combinations of $L_1$ and $L_2$ of $M_1$ and $M_2$.

In Fig. 5, the simulated values of threshold voltage as a function of channel length are compared with those of the model values. It is seen that the threshold voltage rolls-up with decreasing channel lengths for a fixed $L_1$. This happens due to the increased $L_1/L_2$ ratio at decreasing channel lengths since the portion of the larger work function gate is increased as the channel length reduces. This unique feature of the DMG structure is an added advantage when the device dimensions are continuously shrinking. From the results it is clearly seen that the calculated values of the analytical model tracks very well the simulated values. The threshold voltage values show a small difference between the two. This difference is attributed by the neglect of the inversion layer charge at threshold at the front interface.

Fig. 6 shows the threshold voltage variation against different channel lengths with body bias $V_B$. In case of DMG-SOI MOSFET, the threshold voltage variation is quite less when compared with SMG-SOI MOSFET. In Figs. 7(a) and (b), the threshold voltage for both DMG and SMG is shown for different body biases for two different channel lengths. In Fig. 7(a) when channel length $L = 0.2$ lm the threshold voltage variation in DMG is smaller than that of SMG. However in Fig. 7(b), when the channel length is reduced to $L = 0.1$ lm, the variation of threshold voltage between for both the cases is same. The threshold voltage saturates as the negative body bias is increased for both DMG and SMG. This condition is achieved for low body bias when the channel length is reduced. For SMG-SOI MOSFET, the shift in the position of the minimum surface poten-

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**Fig. 6.** Threshold voltage variation versus channel length at a body bias of $V_B = -V_T$ with $L_1$ constant at 0.05 lm. The parameters used are: $t_{ox} = 2$ nm, $t_b = 450$ nm, $t_{si} = 100$ nm and $N_A = 1 \times 10^{18}$ cm$^{-3}$.

**Fig. 7.** (a) Threshold voltage variation versus body bias $V_B$ with a channel length $L = 0.2$ lm ($L_1 = 0.05$ lm, $L_2 = 0.15$ lm). The parameters used are: $t_{ox} = 2$ nm, $t_b = 450$ nm, $t_{si} = 100$ nm and $N_A = 1 \times 10^{18}$ cm$^{-3}$. (b) Threshold voltage variation versus body bias $V_B$ with a channel length $L = 0.1$ lm ($L_1 = 0.05$ lm, $L_2 = 0.05$ lm). The parameters used are: $t_{ox} = 2$ nm, $t_b = 450$ nm, $t_{si} = 100$ nm and $N_A = 1 \times 10^{18}$ cm$^{-3}$. 
5. Conclusions

The effectiveness of the dual-material-gate concept to the partially depleted structure has been examined for the first time by developing a 2-D analytical model. The results obtained have been compared with MEDICI simulations. The model results agree well with the simulated results. It also emphasizes that the DMG structure in partially depleted SOI MOSFETs leads to a reduced short channel effects as the surface potential profile shows a step at the interface of the two metals. Thus the short channel behavior of the PD SOI MOSFETs is further enhanced with the introduction of the DMG structure over their single gate counterparts.

References