A 3.3V Compatible 2.5V TTL-to-CMOS Bidirectional I/O Buffer

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Abstract
Design of a 3.3V compatible 2.5V TTL-to-CMOS bidirectional I/O buffer is proposed. Gate oxide protection was implemented without active voltage degradation, which reduces static and dynamic current levels and improves noise immunity for the low voltage circuit of this kind. Fast removal of stored charge further improve gate oxide protection and circuit recovery from overvoltage condition. Circuit was designed and simulated in 0.25\m technology.

1. Introduction

With power reduction as a driving force the supply voltage for VLSI circuits has reduced from 3.3V to 2.5V, but still not all the components are available in 2.5V technology. In this transition scenario a trade-off between cost, performance, and power consumption demands for a mixed voltage system in which both the 2.5V and 3.3V components are interfaced to the common system bus. In these mixed voltage systems 2.5V components will be driven by 3.3 V components at their inputs and vice-versa [1-3].

There are two potential problems relating to large leakage current and gate oxide protection in these mixed voltage interface components [1-3]. Consider the case of conventional 2.5V I/O buffer driven by 3.3V signal as shown in FIG.1. A 3.3V voltage level at the PAD will see two current conducting paths as marked, shorting the two different power supplies through system bus. This loading by the system bus is a source of undesired power consumption and may damage the circuit as well. This also degrades the voltage level at the system bus. For the voltage reduced technology, gate oxide thickness also reduces. This makes the gate oxide more vulnerable to overvoltage induced stresses due to high voltage across it. Overvoltage condition (at PAD) refer to the voltage levels of 3.3V or higher at the PAD and referred so throughout the discussion. The constraint of limited stress of gate oxide and MOS transistor requires that no terminal pair voltage of MOS transistor exceeds 2.5* 0.2V.

In this paper design of a 2.5V bidirectional I/O buffer is proposed which overcomes these problems.

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the circuit. The I/O buffer is designed to function as input only or output only or bidirectional buffer in mixed voltage environment without introducing hazards and altering functionality.

2.1. Input buffer

Input buffer has bus hold path in it, controlled by bushold enable control signal. Bushold path was introduced to ensure that input to input buffer never floats. In the input buffer’s circuit all the PMOS transistors, with their S/D terminal connected directly to PAD voltage, have their n-well floating. This floating n-well voltage is generated by the stack of four PMOS transistors PF5-8 [4] (see FIG2).

The overvoltage condition at the PAD is sensed against the PMOST PF1, whose gate (node VDT) voltage is at Vcc or Vcc-Vtn depending on whether output buffer is OFF or ON (i.e. ’oe’ is HIGH or LOW). This defines the overvoltage detection threshold. NMOS transistor N3 (and similarly N4, PMOS transistors P2, P3) is(are) introduced to satisfy the constraint of terminal pairs voltage less than Vcc 0.2V for MOS transistor. Overvoltage condition at PAD is latched as HIGH in the latch formed by inverters IL1, IL2 and pass transistor PT1 with inverter IB1. This pulls down the gate voltage level and thus turns NMOS transistor N5 OFF, now gate voltage of PMOST in pass gate PT2 starts following the PAD voltage via PF3. This cuts off the direct path from PAD to input of input buffer. Still the true logic voltage level at the input of the buffer is maintained by transistor PF4 which is controlled by inverter IB3 and PMOS transistor P3. Thus both the problems of leakage current through bushold path of input buffer and overvoltage across the gate oxide are avoided. This circuitry which is designed to detect the overvoltage condition at the PAD and generate appropriate signals/voltages is referred as the ‘overvoltage detection circuit’.

2.2. Output buffer

Output buffer was designed to have three different drive strengths, controlled by two control bits.
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FIG3: Charge removal circuit

Overvoltage detection circuitry along with the design of control logic is used to prevent the high leakage current path in output driver PMOS transistor. Upper part of FIG. 2, gives the logical schematic for the output buffer with control circuit. In the output driver cascode of two NMOS transistors (NO1 and NO2) is used to reduce the stress voltage on the NMOS transistor NO2. NMOST NO5 also serves the similar purpose. In the overvoltage condition at PAD, gate of transistor PF01 will follow the PAD voltage through the PF02, turning PF01 off. PMOST PF03 also turns off in this case.

In the overvoltage condition at PAD, charge is stored at various nodes in the overvoltage detection circuit. This stored charge slows down the process of circuit’s recovery from the overvoltage condition and also causes stress condition for the transistors. Charge removal circuitry is designed to help in otherwise slow residual charge removal process from various nodes, as soon as PAD comes to the normal condition from overvoltage condition. FIG. 3 gives the schematic of charge removal circuit function of which is self explanatory and evident from figure. This provides appropriate feedback to remove residual charges fast. Block diagram of the proposed complete I/O buffer is shown in FIG. 4. This can be seen as made of three distinct parts:

1. Overvoltage detection circuit,
2. Input Buffer with bus hold path, and
3. Output Buffer including the predriver and driver.

3. Simulation Results

The I/O cell area was 84x210(1 m² in 0.25µm technology. Input buffer was designed to achieve the \( V_{IH} = 2.0V \) and \( V_{IL} = 0.8V \) with delays of ~640ps for minimum sized inverter as load. For output buffer \( t_{PLH} \) and \( t_{PHL} \) were 1.58ns and 1.4ns respectively for a load of 30pF.

To verify that no large leakage current path occurs in the proposed I/O buffer the PAD voltage is forced to overvoltage condition and current drawn from the input terminal is monitored. Simulation result is shown in FIG. 5, which shows/confirms a negligible drawn current (<1µA) from the PAD in overvoltage condition at PAD. Due to the response delay of the overvoltage detection circuit to high voltage condition at PAD a small transient current peak is observed at node 'in1'.

To verify that the circuit meets all the requirements with respect to the gate oxide protection, all the critical transistors in the circuit, which can potentially face the gate oxide stresses, are identified and checked for meeting the restriction of terminal pairs voltage of less than \( V_{CC} \times 0.2V \). Overvoltage at the PAD and thus gate oxide stresses results in \( V_{t} \) shift due to gate oxide damage. As a rule of thumb a device is no longer good if \( V_{t} \) shifts by more than 25mV. Time period for this depends on the integral of gate oxide stress over a period of time. Qualitatively a typical case of rising overvoltage pulse at the PAD and the voltage across the gate oxide is shown in FIG.6a, voltage across the gate oxide tends to rise along with the PAD until the overvoltage detection circuit comes in to action. Once the overvoltage detection circuit becomes effective, voltage across the gate oxide will settle down to the
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FIG.5 Floating well voltage and input buffer's input voltage in overvoltage condition

Vcc. This figure shows a typical static case. Since for 2.5V technology maximum Vcc is 2.7V, many of the transistors in circuit can face this voltage across the gate oxide for long time and this is guaranteed by the technology. The shaded area in the FIG.6a shows this and is guaranteed by the technology. If the shaded area in FIG.6a is less than shaded area in the FIG.6b then the gate oxide is protected for a given technology. For the present circuit the most critical transistors in regard to gate oxide protection are input buffer's NMOSTs, which face the voltage at terminal ‘in1’ across their gate oxide. The average voltage stress across gate oxide for one cycle of data toggling is found for these transistors for 3.3V/ns rising overvoltage pulse of 50MHz and is verified that the criterion for gate oxide protection is satisfied.

4. Summary

Design of a 2.5V TTL-to-CMOS bidirectional I/O buffer is presented, which can work in mixed voltage environment without introducing the hazards of high leakage current and gate oxide stress. This design doesn't use any technological solutions and is designed for standard CMOS process technology.

5. References