A Simple Fast Voltage Controller for Single-Phase PFC Converters

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Abstract - In this work a simple and robust voltage controller is proposed to improve voltage dynamics in the Power Factor Corrected (PFC) converters. The proposed controller eliminates twice the line frequency ripples from the voltage feedback path allowing large bandwidth design of voltage loop controller. As the voltage ripple is cancelled without any filtering, the controller action can be exercised at frequencies comparable to switching frequency. This eliminates large overshots and undershoots during transients, which are common in conventionally designed PFC converters. The design of the proposed controller is described and simulation results are presented to demonstrate the feasibility of the proposed technique.

I. INTRODUCTION
Motivated by stringent power quality regulation and strict limits on the Total Harmonic Distortion (THD) of input current, the research in improved power quality utility interface has gained considerable importance. AC-DC Boost PFC converter (Fig. 1) employing active wave shaping techniques for power factor correction has been found to be an optimal solution in terms of cost, efficiency and power density [1].

In these converters, presence of the twice the line frequency ripple on the DC link voltage and its subsequent propagation into the feedback signal results in significant distortion of the input current reference leading to high total harmonic distortion in the input current [1]. The voltage loop regulator is therefore designed with bandwidth in the range of 10-20 Hz, to negate the effect of the low frequency ripples in the feedback loop. This leads to slow voltage regulation with transients lasting for several line cycles. Several techniques [2-8] have been proposed to provide fast voltage regulation in the PFC converters. These techniques essentially involve filtering or cancellation of the feedback ripple.

The feedback ripple cancellation techniques [2-6] overcome bandwidth limitations placed by low pass filtering. In these techniques, the feedback ripple is estimated using a mathematical model of the system and cancelled. As no filtering is required, the voltage controller action can be exercised at frequencies comparable to switching frequency rather than line frequency. However, since these techniques are based on a model of the system, they require precise estimation of the DC link capacitance as well as the use of an additional output current sensor. Moreover, these techniques are not readily extendable to other PFC topologies.

Improved filtering techniques such as notch filters [7] and sample-and-hold methods [7,8] provide simple control schemes, which can be easily integrated into conventional PFC control scheme. These techniques provide a limited improvement in DC bus voltage dynamics by increasing the regulation bandwidth to 50-100 Hz.

In the present work a novel feedback ripple cancellation technique is proposed. Key features of the proposed algorithm are
• No additional sensors
• Easily extendable to other PFC topologies
• Insensitive to parameters such as capacitance

Additionally proposed fast controller overcomes the voltage bandwidth limitations posed by the conventional PFC controller design by effectively canceling twice the line frequency ripples in the feedback path.

II. DESIGN OF FAST CONTROLLER

Design of fast controller is divided in two parts. The first part deals with development of ripple estimation algorithm and the second part involves design of large bandwidth voltage regulator.

A. Ripple Estimation
Conceptually estimation of ripple on the DC bus voltage requires estimation of the ripple magnitude and then multiplication of this magnitude with the shape of the ripple [2,3,5]. The ripple component of the DC bus voltage is found to be [3]

$$v_{\text{rip}}(t) = I_o \sin(4 \pi f_L t) \left(1 - \frac{I_o}{I_L}ight)$$

Here $v_{\text{rip}}(t)$ is the voltage ripple, $I_L$ is line frequency and $I_o$ is the output current.
From eqn (1) estimated ripple voltage \( v_{\text{cst}}(t) \) can be given as
\[
v_{\text{K}}(t) = -K_r \sin(4\pi f_L t) \quad (2)
\]
Where the term \( \sin(4\pi f_L t) \), synchronized to zero crossing of input voltage, is the shape of the voltage ripple and \( K_r \) is the magnitude of the ripple.

Peak values of sinusoidal signals can be found by sampling the signal at zero crossing of another sinusoidal signal phase shifted by \( \pi/2 \) radians. Using this method the peak value of the ripple is found to be:
\[
'\text{ripp}' = |S(n)| - |S(n-1)| = 2K_r \quad (3)
\]
The peak to peak value of the ripple can be found by sampling the signal at zero crossing of another sinusoidal signal phase shifted by \( \pi/2 \) radians. Using this method the peak to peak value of the ripple is found to be:
\[
\text{ripp}_P = |S(n)| - |S(n)| = 2K_r \quad (4)
\]

### B. DC Voltage Controller

The block diagram of the proposed fast controller is shown in Fig. 2. Sensed DC bus voltage \( v_o(t) \) comprises of averaged value \( V_0 \) and ripple \( v_{\text{ripp}}(t) \) as:
\[
v_o(t) = V_0 + v_{\text{ripp}}(t) \quad (6)
\]

The averaged component \( V_0 \) is fed to the PI voltage controller for zero error DC bus voltage regulation and distortion free current reference. \( V_0 \) is obtained by subtracting estimated ripple voltage \( v_{\text{ripp}}(t) \) from the sensed DC voltage \( v_o(t) \) as:
\[
V_0 = v_o(t) - v_{\text{ripp}}(t) \quad (7)
\]

\( V_0 \) is compared with set reference voltage \( V_0^* \). The resulting voltage error \( \text{v}^* \) at the \( n^{th} \) sampling instant is given below.
\[
\text{v}_c(n) = |V_0^* - V_0(n)| \quad (8)
\]

Output of PI voltage regulator \( v_{\text{PWM}}(n) \) at \( n^{th} \) sampling instant is:
\[
v_{\text{PWM}}(n) = v_{\text{PWM}}(n-1) + K_1 \text{v}_c(n) + K_2 \text{v}_c(n-1) \quad (9)
\]

Where \( K_1 \) and \( K_2 \) are the proportional and integral gain constants, \( \text{v}_c^* \) is the error at the \( (n-1)^{th} \) sampling instant. The output of the controller \( v_{\text{PWM}}(n) \) is limited to a permissible value and is taken as an amplitude of the reference supply current \( I_{\text{ref}} \) and is fed to an appropriate current regulator.

![Switching Signal](image)

**Fig. 2** Proposed fast controller for boost PFC converter

### III. RESULTS AND DISCUSSIONS

Digital simulation of the proposed converter system is carried out under varying line and load conditions for a 1kW boost PFC converter to establish the robustness of proposed fast controller. A 1 kHz voltage bandwidth is selected as a compromise between computational requirements and voltage regulation. A PWM current controller is used for this study. Converter and controller parameters are provided in Table I. Dynamics of PFC converter is evaluated under step variation of load from 0.16pu to 1 pu and also under abrupt variations in line voltage from 85Vrms to 270Vrms, which are common in power supply applications.

**Table I Specifications of Proposed Converter**

<table>
<thead>
<tr>
<th>Converter Parameters</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power Rating</td>
<td>1 kW</td>
</tr>
<tr>
<td>Input Voltage</td>
<td>220 VAC</td>
</tr>
<tr>
<td>Output Voltage</td>
<td>400 V</td>
</tr>
<tr>
<td>PWM Frequency</td>
<td>20 kHz</td>
</tr>
<tr>
<td>L_0</td>
<td>1 mH</td>
</tr>
<tr>
<td>C</td>
<td>2200 uF</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>PI Voltage Regulator</th>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Controller Bandwidth</td>
<td></td>
<td>1 kHz</td>
</tr>
<tr>
<td>K_p</td>
<td></td>
<td>1.9</td>
</tr>
<tr>
<td>K_i</td>
<td></td>
<td>0.06</td>
</tr>
<tr>
<td>PI Current Regulator</td>
<td>Parameter</td>
<td>Value</td>
</tr>
<tr>
<td>K_p</td>
<td></td>
<td>0.08</td>
</tr>
<tr>
<td>K_i</td>
<td></td>
<td>0.005</td>
</tr>
</tbody>
</table>

**Fig. 3a** shows dynamics of proposed fast controller based PFC converter. The converter exhibits excellent voltage regulation under severe line and load variations expected in power supply applications. **Fig. 3b** shows comparison of voltage dynamics of proposed fast controller with conventional sample and hold controller [7,8] with a bandwidth of 100Hz. Large overshoots and undershoots common in low bandwidth controller design is completely eliminated by fast controller even under considerable line and load variations.

Delay involved in estimation of ripple magnitude reflects in the THD of input current during transients. However, excellent ripple rejection under steady state can be clearly seen from low input current THD and small 3rd harmonic component (Fig. 3c).
The proposed fast controller overcomes fundamental tradeoff in the PFC design as clearly seen from the simulation results. The THD of input current during steady state is well below the requirements stipulated by the standards while maintaining excellent voltage regulation. Further work includes hardware testing of the proposed design with DSP TMS320F240 and also implementation with analog signal processing for enhancing acceptability of proposed controller.

V.  ACKNOWLEDGEMENT

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VI.  REFERENCES