Investigation of the Novel Attributes of a Fully Depleted Dual-Material Gate SOI MOSFET

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Abstract—The novel features of a fully depleted (FD) dual-material gate (DMG) silicon-on-insulator (SOI) MOSFET are explored theoretically and compared with those of a compatible SOI MOSFET. The two-dimensional numerical simulation studies demonstrate the novel features as threshold voltage roll-up and simultaneous transconductance enhancement and suppression of short-channel effects offered by the FD DMG SOI MOSFET. Moreover, these unique features can be controlled by engineering the workfunction and length of the gate material. This work illustrates the benefits of high-performance FD DMG SOI MOS devices over their single material gate counterparts and provides an incentive for further experimental exploration.

Index Terms—Carrier transport efficiency, dual-material gate (DMG) fully depleted (FD) SOI MOSFET, gate-material engineering, silicon-on-insulator (SOI).

I. INTRODUCTION

During the past decade, CMOS technology has seen excellent high-speed performance achieved through improved design, use of high-quality material, and processing innovations. In order to realize high-speed and high-packing density, MOS integrated circuits, the dimensions of MOSFETs have continued to shrink according to the scaling law proposed by Dennard et al. [1]. However, with the reduction of channel length, an increasing amount of effort is focused to circumvent the “undesirable” short-channel effects (SCEs), which cause the dependence of device characteristics, such as threshold voltage, upon channel length.

In contrast to the bulk device, the front-gate in an SOI device has better control over its active device region in the thin film, and hence charge-sharing effects from source/drain regions are substantially reduced. In addition, thin-film SOI MOSFETs offer superior electrical characteristics over bulk MOS devices such as reduced junction capacitances, increased channel mobility, and excellent latch-up immunity [2], [3]. However, to take advantage of the ameliorated SCEs in fully depleted (FD) SOI, thin-film thickness $t_S$, must be considerably smaller than the source/drain junction depth. Due to the existence of a buried oxide, there exists a strong coupling through the buried oxide in thin-film devices. Consequently, buried oxides much smaller than 100 nm are needed, which trades off with junction capacitance considerations. Moreover, SOI devices continue to have a nonuniform electric field distribution in the channel with the peak of the electric field profile occurring near the drain. Thus, the charge carriers move with a low velocity near the source gradually accelerating toward the drain resulting in a lower mean carrier transport velocity. Another undesirable phenomenon at shorter channel lengths is the hot-carrier effect which is precipitated due to the electric field peak near the drain. Several solutions have been proposed in literature to obviate SCE like Ushiki et al. [4], used tantalum gate to facilitate the adjustment of the threshold voltage of an SOI device without raising the thin-film doping density substantially by taking advantage of the workfunction of tantalum. But this does not improve the carrier transport efficiency. Moreover, in an FD SOI device, choosing an arbitrary metal gate with workfunction close to the band edges would require a high channel doping to meet the off-current specifications. Alternative gate structures such as double-gate (DG) [5] have been proposed to improve the SCE and transconductance of SOI devices. But, since the thickness of silicon between the two gates is smaller than the physical gate length, the most critical lithography step in printing the DG transistor becomes patterning of the thin-film, rather than the physical gate-length patterning [6].

In 1999, Long et al. [7] proposed a new type of FET structure, dual-material gate (DMG) FET, employing “gate-material engineering” instead of “doping engineering” to improve both carrier transport efficiency and SCEs. In a DMG FET, two different materials with different workfunctions are laterally merged together. The work function of metal gate 1 (M1) is chosen greater than metal gate 2 (M2), i.e., $\phi_{M1} > \phi_{M2}$ for an n-channel MOSFET and vice-versa for a p-channel DMG MOSFET. This introduces a potential step in the channel. Thus, the DMG structure achieves simultaneous suppression of SCEs and transconductance enhancement due to the creation of a step in the channel potential profile and a more uniform electric field distribution along the channel.

With SOI rapidly emerging as the technology for next-generation VLSI, the effects of DMG in submicron SOI technology remain to be investigated [8], [9]. In this paper, for the first time we have investigated the efficacy of DMG structure in FD SOI devices using two-dimensional (2-D) numerical simulations. The unique features of the DMG SOI device are explored and compared with those of a single-material gate (SMG) SOI in terms of threshold voltage ($V_{th}$) roll-off, drain-induced barrier lowering (DIBL), on-current ($I_{on}$), off-current ($I_{off}$), and the ratio of transconductance to drain conductance ($g_{m}/g_{d}$) with a purpose of uncovering the potential benefits of the FD DMG SOI MOS structure and its possible integration into the current CMOS technology.
II. FD DMG-SOI STRUCTURE AND ITS PARAMETERS

A schematic cross-sectional view of an n-channel fully depleted DMG SOI MOSFET implemented in the 2-D device simulator MEDICI [10] is shown in Fig. 1 with gate metals M1 and M2 of lengths $L_1$ and $L_2$, respectively. The doping in the p-type body and n$^+$ source/drain regions is kept at $6 \times 10^{16}$ cm$^{-3}$ and $5 \times 10^{19}$ cm$^{-3}$ respectively. Typical values of front-gate oxide thickness, buried-oxide thickness and thin-film thickness are 5, 400, and 50 nm, respectively. The workfunction of gate metals M1 and M2 are chosen as 4.5 and 4.1 eV, respectively. All the device parameters of SMG are equivalent to those of DMG unless otherwise stated.

III. COMPUTER SIMULATION RESULTS

Computer experiments are designed to explore the characteristics of DMG SOI with respect to those of a compatible SMG SOI MOSFET.

The major target parameters for comparison are as follows. The linear threshold voltage ($V_{th, lin}$) is based on the maximum-$g_m$ method (linear extrapolation of $I_D - V_{DS}$ to zero) at $V_{DS} = 0.05$ V. The saturation threshold voltage ($V_{th,sat}$) is based on a modified constant-current method at $V_{DS} = 0.8$ V [11]. The saturation current ($I_{on}$) is the drain current at $V_{DS} = 1$ V. The leakage current ($I_{off}$) is the drain current at $V_{GSS} = 0$ V and $V_{DS} = 1$ V (or $V_{DS} = 0.05$ V, as stated). The transconductance, $g_m$, is extracted from the slope of $I_D - V_{GS}$ at $V_{GSS} = V_{DS} = 0.8$ V. The drain conductance ($g_d$) is extracted from the slope of $I_D - V_{DS}$ between $V_{DS} = 0.75$ V and 1.0 V at $V_{GSS} = 0.8$ V.

A. Performance Comparison With SMG SOI MOSFET

Output characteristics of the DMG and SMG SOI devices are compared for the same channel length $L = 0.2 \mu$m in Fig. 2. The workfunction of the gate metal for SMG SOI is chosen as 4.1 eV. Choosing a body doping as $N_A = 6 \times 10^{16}$ cm$^{-3}$ for the SMG SOI yields a threshold voltage, $V_{th} = -0.050$ V which is not suitable for performance comparison. The body doping of SMG SOI device is thus chosen as $N_A = 3.591 \times 10^{17}$ cm$^{-3}$, which yields the same threshold voltage, $V_{th} = 0.229$ V for both the DMG and SMG MOSFETs.

It is evident from Fig. 2 that the DMG SOI shows a reduction in output conductance compared to the SMG SOI MOSFET. This can be used to realize an increased voltage gain as discussed in Section III-C. This unique feature of the DMG SOI is not easily achievable by doping engineering [12].

To probe the physical mechanisms responsible for the improved performance of the DMG SOI MOSFET, surface electric field and electron velocity profiles across the channel for the DMG and SMG SOI are shown in Fig. 3. In a DMG SOI, the electric-field discontinuity at the interface of the two gate metals (one-half of the channel for gate lengths $L_1$ and $L_2$ chosen) causes the overall channel field to be "flattened" (increased at the source side), resulting in larger average velocity when the electrons enter into the channel from the source. The potential step (field discontinuity) also forces channel field to redistribute mostly at the drain side as the drain bias is increased (from 0.75–1 V). This screening effect is responsible for the observed reduction in DIBL and channel length modulation (CLM). These behaviors will be more pronounced in a DMG with lower channel doping, in which electron transport efficiency will be more pronounced as a result of enhanced electron mobility and velocity in most of the channel. Also shown in Fig. 3 are the comparisons with SMG SOI device having body doping same as that of the DMG SOI MOSFET. It is evident from the figure that the enhanced source-side electric field leads to an increased electron velocity in the channel for a DMG SOI device.

B. Scaling Characteristics at a Fixed $L_1$

Scaling characteristics are studied for different values of the metal M1 (length $L_1$), with all other parameters taking their nominal values. The most significant improvement over the SMG SOI is the $V_{th}$ roll-up for the DMG SOI device as shown in Fig. 4. With the proper control over gate metal M1 (length $L_1$), threshold voltage will not be sensitive to the gate length, a desirable feature in deep-submicron technology. The $V_{th}$
roll-up is due to an increase in the portion of larger workfunction gate M1, i.e., increase of $L_1/L_2$ ratio as $L$ decreases (at fixed $L_1$). The gate M1 is the main control gate whereas M2 serves as the screen gate and with increasing $L_1/L_2$ ratio as $L$ decreases, $V_{th}$ increases. The $V_{th}$ roll-up also leads to a lower $I_{off}$ for the DMG SOI MOSFET.

C. Effect of $L_1/L_2$ Ratio at a Fixed Channel Length $L$

At a fixed channel length $L = L_1 + L_2$, the location of the potential step can be tuned for different values of the $L_1/L_2$ ratio. This feature is investigated with $L_1$ ranging from 0 (SMG) to 0.15 μm at a fixed $L = 0.2$ μm for the target parameters of $V_{th,lin}$, $V_{th,sat}$, $V_{DIBL}$, $I_{off}$, $g_m$, $g_d$, and $g_{m/d}$.

It is observed from Fig. 5 that as $L_2$ increases ($L_1/L_2$ increases), threshold voltage increases. This leads to a lowering of $V_{DIBL}$ and a consequent reduction in the influence of drain electric field on the channel. It is observed from the figure that as $L_2$ approaches the total channel length $L = L_1 + L_2$, $V_{DIBL}$ increases and the device begins to operate as a SMG with higher gate workfunction. This illustrates the desirable feature of the DMG structure in suppressing DIBL. However, as $L_2$ increases therefore, $L_1/L_2$ increases, saturation current decreases although leakage current also decreases as shown in Fig. 6. This is mainly due to the elevated threshold voltage at increasing $L_1$.

As shown in Fig. 7(a), it is seen that as $L_2$ increases the drain conductance, $g_d$, continues to decrease. With a larger portion of the channel being “screened” by the gate M1, the influence
of drain bias upon the channel current reduces. Fig. 7(a) also shows the variation of transconductance, $g_{m}$, in saturation, for different values of $L_1$ in a fully depleted DMOS SOI MOSFET. It is observed that $g_{m}$ is higher for a DMOS SOI as compared to the SMG ($L_1 = 0$). However, with $L_1 \rightarrow L$, it theoretically leads to an SMG SOI with a larger workfunction, consequently, $g_{ds}$ increases and $g_{m}$ decreases as the gate overdrive decreases due to elevated threshold voltage. Fig. 7(b) shows the variation of voltage gain, $g_{m}/g_{ds}$ as function of M1 gate length, $L_1$.

It is observed from Figs. 5–7 that the optimum ratio of gate metal lengths, $L_1$ and $L_2$, for both logic and analog circuits application is $L_1/L_2 = 1$. With $L_1/L_2 = 1$, we get a reduced DIBL, lower off-state current, higher $g_{m}$, increased on-state current, $I_{on}$ (for devices with same threshold voltage), and a higher voltage gain, $g_{m}/g_{ds}$, in comparison to a SMG SOI MOSFET. This conclusion is further strengthened by observing the simulations done for a channel length $L = 0.3\mu m$ DMOS SOI MOSFET. It is seen from Figs. 5–7 that a gate length ratio $L_1/L_2 = 1$ is most beneficial for VLSI circuit applications. This result is significant in light of a gate-length ratio $L_1/L_2 = 1/2$ proposed for a HMG-FET [13] because with device design already in sub-100 nm regime, realizing $L_1/L_2 = 1$ is more amenable from a photolithographic viewpoint.

**D. Effect of Workfunction Difference ($\Delta W$) at a Fixed Channel Length $L$**

At a fixed ratio of gate metal lengths $L_1/L_2 = 1$, the effect of metal M1 workfunction on the performance of the DMOS SOI MOSFET is studied by varying its values. The workfunction of metal M2 is kept fixed at 4.1 eV. The results are shown in Figs. 8–10. It is observed from Fig. 8 that with increasing workfunction difference, $\Delta W$, threshold voltage increases for the same $L_1/L_2$ ratio. Nevertheless, choosing a high $\Delta W$ leads to a prohibitively large threshold voltage unsuitable for sub-quarter micron devices working at scaled supply voltage. On/off-state currents also exhibit behavior similar to the $L_1/L_2$ ratio variation as shown in Fig. 9. As a result of increased $V_{th}$ at increasing $\Delta W$, $I_{off}$ as well as $I_{on}$ decrease. A workfunction difference, $\Delta W$, of 0.4 eV results in nearly 25% increment in on-current, $I_{on}$, for a DMOS SOI device over the conventional SOI MOSFET with equivalent threshold voltage ($I_{on} (DMOS) = 0.362\ mA$ and $I_{on} (SMG) = 0.291\ mA$). Increased $\Delta W$ (i.e., larger potential step at the metal gate interface) also favors $g_{m}$ reduction as shown in Fig. 10. Whereas $g_{m}$ decreases after $\Delta W = 0.4\ eV$ due to reduced overdrive voltage available at the elevated threshold voltage for a fixed gate bias.

This work has thus demonstrated the superior performance of the FD DMOS SOI MOSFET over their SMG counterparts for
VLSI circuit realization and the optimum parameters have also been investigated. Moreover, the investigation elucidates an alternative way of achieving high-performing DMG SOI devices by virtue of "gate material engineering."

IV. CONCLUSION

The novel properties of fully depleted DMG SOI MOSFETs have been studied in the context of their potential integration in the current CMOS technology. The unique features of the DMG that are not easily available in the conventional SOI devices include: $V_{th}$ roll-up, reduced DIBL, and simultaneous transconductance enhancement and SCE suppression. They can be controlled by an alternative way of gate material engineering. Numerical simulations indicate an optimum gate-length ratio $L_1/L_2 = 1$ and a workfunction difference $\Delta W = 0.4$ eV for a FD DMG SOI MOSFET.

One of the difficulties in integrating DMG structure in the present CMOS technology maybe its asymmetric structure, but Zhou [13] suggested two fabrication procedures requiring only one additional mask step. Moreover, the proposed FD DMG SOI MOSFET may also be employed in symmetric structures (like an LDD spacer). With the CMOS processing technology already into the 100-nm regime [14], fabricating sub-100-nm feature gate lengths should not preclude the possibility of realizing the substantial performance gains over conventional SOI devices and excellent immunity against SCEs that the DMG SOI MOSFET promises.

REFERENCES


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