General Rules for Signal Flow Graph Modeling and Analysis of DC-DC Converters

MUMMADI VEERACHARY, Member, IEEE
Indian Institute of Technology Delhi

Signal flow graph (SFG) nonlinear modeling approach is well known for modeling dc-dc converters. However, all possible SFGs of a given dc-dc converter system will not yield the generalized graph. A systematic procedure and guidelines for developing unified flow graph models of the dc-dc boost converters, from which complete behavior can be determined is presented. Usefulness of the proposed method is demonstrated through examples. As an illustration a 2-cell cascade boost and interleaved boost converter systems are taken as examples. Derivation of large, small-signal and steady-state models from generalized flow graph is also demonstrated. Large-signal model is developed and programmed in TUTSIM simulator. Large-signal responses against supply and load disturbances are obtained. Experimental observations are provided to validate the proposed algorithm.

I. INTRODUCTION

Switch-mode dc/dc converter has evolved into an essential component in the electronic equipment [1] and finding widespread applications in computers, battery chargers, solar cell based power converters used in space power conditioning systems, etc. The wide variety types of converter topologies have been developed by different researchers to cater predefined needs. These include simple basic converters such as buck, boost, and buck-boost, isolated converters, complex converters such as cascade, interleaved converters, etc. Cascade converters with new control strategies is coming up to increase the power processing capability of the power electronic system. Particularly, aeronautics and telecommunication appliances require large/smaller conversion ratios. These requirements can be fulfilled either with the help of isolated step-down/step-up PWM (Pulse Width Modulated) dc-dc converters or nonisolated converters. However, the use of step-down/step-up converters with transformers, isolated converters, results in large switching surges that may damage the switching devices [2–3]. Further, use of transformer limits the switching frequency of the converter. An alternative option, for realizing larger/smaller dc conversion ratios, is cascading of the converters [4]. This scheme mainly uses multistage approach that consists of n-basic converters connected in cascade. Instead of cascading the basic dc-dc converter cells they can also be connected in parallel and controlled in an interleaved fashion, which increases the reliability of the converter system and reduces the size of filtering components [5]. However, in either case modeling of the converters will become difficult with increasing number of cells.

State-space averaging method is the most popular approach used for modeling of the dc/dc switching converters [6]. However, this method is sometimes tedious, especially when the converter circuit contains a large number of elements. Furthermore, the linearized models do not predict the large-signal stability information, and are only sufficient to predict small-signal stability. Large-signal models are proposed, but these models do not provide a generalised model, which will predict the complete behavior of the circuit. To overcome some of the problems mentioned above, a signal flow graph (SFG) nonlinear modeling method was developed for PWM converters [7–9]. The advantages of this method are: 1) it converts the switching converter (two or multistate) into a unified dynamic model, 2) from unified model, it is possible to derive large, small-signal and steady-state models with minimum mathematical manipulations, 3) it provides the designer an easy way of getting large-signal global behavior when it is combined with TUTSIM simulator, and 4) it is possible to derive various
relationships among the circuit variables without any difficulty, particularly small-signal transfer functions.

However, the SFG method has so far been applied only for simple converters like buck, boost, and buck-boost converters, etc. Furthermore, there are no prescribed guidelines while drawing the flow graphs for the dc-dc converters. In this paper, general rules to be followed while developing the SFGs for the dc-dc converter are given and then applied for analysis of complex dc-dc converter systems. Unified SFG models are developed for cascade boost and interleaved boost converter systems. Derivation of large, small-signal, and steady-state models from the unified SFG models is demonstrated for two different converter systems, namely, 2-cell cascade boost, interleaved boost systems. Theoretical, simulation and experimental results are given to substantiate the SFG modeling of the dc-dc converters.

II. GENERAL RULES FOR DRAWING SFGS

The following generalized algorithm must be followed for drawing the SFGs of the dc-dc converter systems.

Step 1 The sequence of nodes is in the sequence of elements, inductor or capacitor, appearing in the circuit. Improper sequence of nodes results a graph in which the number of closed loops and forward paths different from the true graph.

Step 2 While drawing the SFGs voltage node first and then current node should be indicated for inductive elements. For capacitive elements current node first and then voltage node should follow.

Step 3 Individual loops must be considered while writing down the circuit loop voltage equations using KVL.

Step 4 While using KCL at junction points shunt branch currents always must be expressed in terms of other currents.

Step 5 The capacitive voltage nodes are connected to the preceding intermediate inductive branch nodes either with a forward path transmittance of -1 or with a switching function. The path transmittance -1 or switching function corresponds to the boost or buck mode of operation of the converter, respectively.

Step 6 Each capacitor current node is connected from its preceding inductor current node. Again the path transmittance -1 or switching function corresponds to the boost or buck mode of operation of the converter, respectively.

Step 7 The source current node is a sink node and receives signals from all those inductors which are having a common terminal with the source. The path transmittance -1 or switching function depends on the boost or buck mode of operation of the converter.

Step 8 The number of switching functions, \(K_1, K_2, \ldots, K_n\), where \(n\) is number of operating modes, \(2, 3, \ldots, N\), depends on the number of operating modes of the circuit.

Step 9 In the simplified SFG, using algebraic flow graph rules, the closed loops mainly forms with the inductive and capacitive branch nodes.

In the following sections SFG development, for two different converter systems, is discussed and it uses the following assumptions:

1) Switching elements of the basic converter cells are assumed to be ideal.
2) The individual cells of the dc-dc converter system operate in the continuous inductor current mode.
3) The switches operate in the predefined fashion.
4) The equivalent series resistance (ESR) of the capacitance and stray capacitances are neglected.
5) Passive components \(R, L, C\) are assumed to be linear time-invariant.

III. DEVELOPMENT OF UNIFIED SFG MODEL FOR N-CELL CASCADE BOOST CONVERTER

This section describes SFG development of dc-dc cascade boost converters consisting of identical/non-identical basic converter cells. In general case many different types of converters can be cascaded to realize the predefined requirements. However, cascading of basic converter cells such as buck or boost converters is the common practice in order to achieve smaller or larger conversion ratios, respectively. When such cascade converters are required to construct, then it is essential to model the converter system both for designing and controller implementation. Particularly, for controller design one has to know the small-signal transfer functions of the converter system. As already mentioned, if the cascade converter system contains more of the stages then transfer functions derivation is really a complex task. An SFG approach is proposed in this section to solve some of the above problems involved in modeling cascade converters using conventional methods. For demonstration of SFG modeling of cascade converters, an \(N\)-cell cascade boost converter system is considered, as shown in Fig. 1, in the first step and a general discussion to obtain all the models (large, small-signal and steady-state) from the unified model is given in subsequent sections. In the second stage the method is extended to model the 2-cell cascade boost converter systems.

It is assumed that the individual boost cells operate in the continuous inductor current mode and the switches \(S_1, S_2, \ldots, S_n\) are synchronized in their operation. This assumed switching sequence results in two modes (mode-1, mode-2) of operation in one cycle time period thus resulting in two switching functions \(K_1\) and \(K_2\). This fact is in agreement with Step 8 of the proposed algorithm given in Section II. During the time \(0 < t < t_{ON}\), mode-1, the
switches $S_1, S_2, \ldots, S_n$, and during $t_{ON} < t \leq T$, mode-2, the diodes $DD_1, DD_2, \ldots, DD_n$ are, respectively, conducting and thus generating two different ON and OFF subcircuits. The converter switches between these two subcircuits, which are linear and a linear system theory can be extended. Considering the switch $\delta$ operation as reference, SFGs $G_{ON}, G_{OFF}$ are generated for ON, OFF subcircuits respectively sharing common nodes and part of the branches. Systematic algorithm given in Section II is used while drawing the SFGs, $G_{ON}$ and $G_{OFF}$. The two SFGs $G_{ON}, G_{OFF}$ are combined to form a simplified SFG. While merging the two SFGs, $G_{ON}$ and $G_{OFF}$, into a single graph $G$, some of the branches exist in the two graphs and some may not. Branches that exist in $G_{ON}$ but not in $G_{OFF}$ are replaced by $K_1$ branches, and the branches that exist in $G_{OFF}$ but not in $G_{ON}$ are replaced by $K_2$ branches. The resulting graph topology, can be mathematically written as

$$G = K_1 G_{ON} + K_2 G_{OFF}$$

where $K_1, K_2$ are the switching functions, whose values depend on the switching times, defined by the following expressions

$$K_1 = \begin{cases} 1 & \text{for } 0 < t \leq t_{ON} \\ 0 & \text{for } t_{ON} < t \leq T \end{cases}$$

$$K_2 = \begin{cases} 0 & \text{for } 0 < t \leq t_{ON} \\ 1 & \text{for } t_{ON} < t \leq T \end{cases}$$

Employing the above switching functions and the two SFGs, $G_{ON}$ and $G_{OFF}$, a unified SFG is generated as shown in Fig. 2. This is a unified SFG of an $N$-cell cascade boost converter system, from which complete behavior, dynamic and steady-state, of the system can be obtained. Systematic procedures for developing the large, small-signal and steady-state models, from this unified SFG, are illustrated in the following sections.

A. Large-Signal and Steady-State Models

Assuming filter corner frequency is much smaller [5] than the switching frequency, the effective signals carried at the outputs of $K_1, K_2$ branches having an average values $d_1(t), d_2(t)$, respectively, are

$$y(t) = x(t)d_1(t)$$

$$y(t) = x(t)d_2(t)$$

Equations (4) and (5) indicate that the output signal $y(t)$ from the switching branches $K_1, K_2$ are the product of the input signal and the duty ratio control signal $d_1(t)$ or $d_2(t)$. From these equations the large-signal models for switching branches are developed. Incorporating these large-signal models for the switching branches in the graph $G$ results a large-signal SFG. This large-signal model can be directly entered into the TUTSIM simulator to study its large-signal behavior.
From the large-signal switching branch models the steady-state switching branch models are derived. In the steady-state, $K_1$ branch will have a transmittance of $m_1(t) = D_1$ and $K_2$ branch will have a transmittance of $m_2(t) = D_2$. Simplifying the large-signal SFG with the above steady-state switching branch models and setting complex frequency $s = 0$, a steady-state model is obtained. From this switching flow graph various steady-state relations can be derived.

B. Small-Signal Model

A small-signal SFG for the N-cell cascade boost converter system can be obtained from the generalized SFG, Fig. 2, by replacing the switching branches ($K_1$, and $K_2$) with their corresponding small-signal equivalent models. For illustration, small-signal equivalent is derived for switching branch $K_1$ in the following lines. For this switching branch the input and output signals are related as

$$y(t) = x(t)\hat{d}_1(t). \quad (6)$$

Letting $X,Y,D$ be the operating point and $\hat{x}(t), \hat{y}(t), \hat{d}_1(t)$ be the corresponding small-signal perturbations satisfies $x(t) = X + \hat{x}(t), y(t) = Y + \hat{y}(t), \hat{d}_1(t) = D_1 + \hat{d}_1(t)$. Inserting these relationships in (6) results in the following equation

$$Y + \hat{y}(t) = (X + \hat{x}(t))(D_1 + \hat{d}_1(t))$$

$$= XD_1 + D_1\hat{x}(t) + X\hat{d}_1(t) + \hat{x}(t)\hat{d}_1(t). \quad (7)$$

Substituting the condition for operating point, which is $Y = XD_1$, and on the assumption of neglecting second-order perturbations ($\hat{x}(t)\hat{d}_1(t)$), the small-signal switching equation for $K_1$ branch is

$$\hat{y}(t) = D_1\hat{x}(t) + X\hat{d}_1(t). \quad (8)$$

On similar lines the small-signal switching branch equation for $K_2$ branch can be derived and it is

$$\hat{y}(t) = D_2\hat{x}(t) - X\hat{d}_2(t) \quad (9)$$

where $D_1,D_2$ are the duty ratios control functions of mode-1, and mode-2, respectively. The above equations define the graphical representation of small-signal switching branches. Upon substitution of the above small-signal switch branches in Fig. 2, and on simplification a small-signal SFG can be generated. This small-signal model, can be used to derive all the small-signal performance transfer functions between any two nodes for frequencies up to about half of the switching frequency $f_s$.

The above generalized treatment is valid for an $N$-cell cascade boost converter system. To validate the above model and to receive large, small-signal, and steady-state models from the unified SFG, a simple 2-cell cascade boost converter is considered in the following sections. However, developing the SFG for 3 and more cells cascade boost converter should be quite similar to the one presented here.

IV. DEVELOPMENT OF SIGNAL FLOW GRAPHS FOR THE 2-CELL CASCADE BOOST CONVERTER SYSTEM

Now the 2-cell cascade boost converter analysis is given adapting the same assumptions as were made in the earlier section. The generalized graph is developed for this converter system using the procedure given in Section II and the corresponding SFG is shown in Fig. 3.

A. Small-Signal Model and Transfer Functions

Adopting the procedure as explained in Section IIIB, a small-signal SFG of the converter is drawn as shown in Fig. 4, where

$$d_k = \frac{k_2V_2}{sL_2 + r_2} - \frac{k_1I_1}{\sigma C_1(sL_2 + r_2)} - \frac{V_1}{(sL_2 + r_2)} - I_2. \quad (10)$$

Various small-signal transfer functions can easily be derived from this graph. However, the following four commonly used transfer functions derivation is given in this section for illustration. The above derivation of input-to-output transfer function is given in the following lines. To start with, various possible forward paths and loops are identified from
the small-signal SFG (Fig. 4). There is only one forward path between the nodes \( \hat{v}_g \) and \( \hat{v}_o \) (\( \hat{v}_o = \hat{v}_{c2} \)).

Its transmittance formed by the nodes (\( \hat{v}_g - \hat{i}_1 - \hat{i}_c1 - \hat{v}_{c1} - \hat{v}_2 - \hat{i}_2 - \hat{i}_c2 - \hat{v}_{c2} \)) is

\[
P_1 = \frac{-Rk_2^2}{sC_1(sL_1 + r_1)(sL_2 + r_2)(1 + sRC_2)}
\]

(11)

In this small-signal SFG three loops are formed by nodes (\( \hat{v}_1 - \hat{i}_1 - \hat{i}_c1 - \hat{v}_{c1} - \hat{v}_1 \)), (\( \hat{v}_c1 - \hat{v}_c2 - \hat{v}_2 - \hat{i}_2 \)), (\( \hat{v}_2 - \hat{i}_2 - \hat{i}_c2 - \hat{v}_{c2} - \hat{v}_2 \)) exist, and their loop transmittances are

\[
\begin{align*}
I_1 &= \frac{-k_1^2}{sC_1(sL_1 + r_1)} \\
I_2 &= \frac{-1}{sC_1(sL_2 + r_2)} \\
I_3 &= \frac{-Rk_2^2}{(sL_2 + r_2)(1 + sRC_2)}
\end{align*}
\]

(12) \hspace{1cm} (13) \hspace{1cm} (14)

The gain between nodes \( \hat{v}_o(s) \) and \( \hat{v}_g(s) \) is obtained by employing Mason’s gain formula [10] given by

\[
\text{Gain} = \sum \frac{P_k \Delta_k}{\Delta}
\]

(15)

where \( P_k \) is the \( k \)-th forward path gain, \( \Delta \) is the determinant of the graph. In this SFG all the loops touch the forward path \( p_1 \) and hence \( \Delta_1 = 1 \).

Applying Mason’s gain formula, the input-to-output transfer function is obtained as

\[
M_o(s) = \frac{\hat{v}_o(s)}{\hat{v}_g(s)} \bigg|_{d(s) = 0} = \frac{P_1 \Delta_1}{1 - (I_1 + I_2 + I_3) + I_1 I_3}.
\]

(16)

Substituting (11)–(14) in the above equation and simplifying results in the following expression

\[
\frac{\hat{v}_o(s)}{\hat{v}_g(s)} = \frac{Rk_2^2}{[\Delta_p + [k_2^2(L_2 s + r_2) + (L_1 s + r_1)](1 + sRC_2) + Rk_2^2C_1(sL_2 s + r_2) + Rk_2^2]}
\]

(17)

where \( \Delta_p = sC_1(sL_1 + r_1)(sL_2 + r_2)(1 + sRC_2) \); \( r_1, r_2 \) are the series resistances of the inductors. The open-loop input impedance is derived as

\[
Z_i(s) = \frac{\hat{v}_g(s)}{i_g(s)} \bigg|_{d(s) = 0} = \frac{\hat{v}_g(s)}{i_g(s)} \bigg|_{d(s) = 0} = \frac{[k_2^2(L_2 s + r_2) + (L_1 s + r_1)](1 + sRC_2) + Rk_2^2C_1(sL_2 s + r_2) + Rk_2^2}{[C_1(sL_2 s + r_2)(1 + sRC_2) + (1 + sRC_2) + Rk_2^2]}
\]

(18)

The open-loop output impedance is

\[
Z_o(s) = \frac{\hat{v}_o(s)}{i_o(s)} \bigg|_{d(s) = 0} = \frac{R(C_1 sL_2 s + r_2)(L_1 s + r_1)}{[\Delta_p + [k_2^2(L_2 s + r_2) + (L_1 s + r_1)](1 + sRC_2) + Rk_2^2C_1(sL_2 s + r_2) + Rk_2^2]}
\]

(19)

The control-to-output transfer function is

\[
T_p(s) = \frac{\hat{v}_o(s)}{d(s)} \bigg|_{l_{ip} = 0} = \frac{V_o(s)}{C_1(sL_2 s + r_2)(L_1 s + r_1)}
\]

(20)

\[
\frac{\hat{v}_o(s)}{d(s)} = \frac{V_o(s)C_1 sL_2 s + r_2)(L_1 s + r_1)}{[\Delta_p + [k_2^2(L_2 s + r_2) + (L_1 s + r_1)](1 + sRC_2) + Rk_2^2C_1(sL_2 s + r_2) + Rk_2^2]}
\]

(21)

The above derived small-signal transfer functions are summarized in Table I.

On the assumption of negligible capacitor ESR the above small-signal transfer functions are derived. However, the ESR of the main filter capacitor has a significant affect on the small-signal dynamics.

Inclusion of ESR will change the small-signal transfer functions and one can easily be determined from the SFG. The SFG of the converter including capacitor ESR is identical to the one shown in Fig. 2 except that the transmittance between the nodes \( i_g \) and \( v_o \) (\( i_{eq}, v_{eq} \)), which is \( R(1 + sRC_1)/[1 + sC(R + R_e)] \) instead of...
TABLE I
Small-Signal Transfer Functions of Converter System

\[
\begin{align*}
\frac{\dot{V}_p(s)}{V_p(s)} &= \frac{\Delta_p + [k_2^2(L_2s + r_1) + (L_1s + r_1)](1 + sRC_2) + Rk_2^2C_1s(L_2s + r_1) + Rk_2^2}{R[C_1s(L_2s + r_1)(L_2s + r_2) + k_2^2(L_2s + r_1) + (L_1s + r_1)]} \\
\frac{\dot{V}_g(s)}{I_g(s)} &= \frac{\Delta_g + [k_2^2(L_2s + r_1) + (L_1s + r_1)](1 + sRC_2) + Rk_2^2C_1s(L_2s + r_1) + Rk_2^2}{[C_1s(L_2s + r_1)(1 + sRC_2) + (1 + sRC_2) + RC_2s]} \\
\frac{V_g(s)}{I_g(s)} &= \frac{V_g(L_2s + r_1) + (L_1s + r_1)(1 + sRC_2) + Rk_2^2C_1s(L_2s + r_1) + Rk_2^2}{C_1L_2k_2s(L_2s + r_1) + (L_1s + r_1)(1 + sRC_2) + Rk_2^2C_1s(L_2s + r_1) + Rk_2^2}
\end{align*}
\]

Fig. 5. Large-signal SFG of 2-cell cascade boost converter.

\(R/(1 + sCR)\) where \(R\) is the ESR of the capacitor.

The dependency of small-signal transfer functions on capacitor ESR is demonstrated for interleaved boost converters in Section V.

B. Large-Signal and Steady-State Models

Adopting the procedure outlined in Section II B the large-signal SFG model is developed and it is shown in Fig. 5. This model is directly entered into the TUTSIM simulator to study its large-signal behavior.

The detailed discussion of large-signal behavior is given in the next section. From the large-signal switching branch models the steady-state switching branch models are derived. In the steady-state, \(K_1\) branch will have a transmittance of \(m_1(t)\) = \(D_1\) and \(K_2\) branch will have a transmittance of \(m_2(t)\) = \(D_2\).

Simplifying the large-signal SFG with the above steady-state switching branch models and setting complex frequency \(s \rightarrow 0\), a steady-state model is obtained. From this switching flow graph various steady-state relations can be derived. Adapting a similar procedure, as outlined in the preceding section, various relationships among the state variables are obtained and they are given for ready reference in Table II.

The above performance characteristics (small-signal transfer functions, steady-state expressions) tabulated in Tables I and II are derived from SFG method. These expressions are in agreement with those obtained from state-space averaging method.

\[\begin{array}{c|c}
\hline
V_0 & \frac{Rk_2^2}{(k_2^2 + r_1 + Rk_2^2)} \\
V_f & \frac{1}{(k_2^2 + r_1 + Rk_2^2)} \\
I_f & \frac{k_2^2}{(k_2^2 + r_1 + Rk_2^2)} \\
V_g & \frac{Rk_2^2}{(k_2^2 + r_1 + Rk_2^2)} \\
\hline
\end{array}\]

V. UNIFIED SIGNAL FLOW GRAPH MODEL FOR AN N-CELL INTERLEAVED BOOST CONVERTER SYSTEM

In this section we develop a unified SFG model for an N-cell interleaved boost converter system. This converter system consists of \(N\) number of basic boost cells connected in parallel, as shown in Fig. 6, and are operating in an interleaved fashion. The following SFG development uses same assumptions as mentioned in Section II except that ESR of the capacitor is taken into account in this case. Here the switching devices \(S_1, S_2, S_3, \ldots, S_N\) operate in an interleaved fashion with a phase shift of \(2\pi/N\) among the converter control signals and the switching sequence is \(S_1, S_2, \ldots, S_{N-1}; S_2, S_3, \ldots, S_N; S_3, S_4, \ldots, S_N, \ldots, S_N\), \(S_1\) so on. This interleaved operating sequence results in \(N\)-modes of operation (Mode-1: \(t_0 < t \leq t_1\), Mode-2:...
Fig. 6. N-cell interleaved converter system.

\[ x_j = \frac{1}{sL_j + r_j}; (j=1, 2, \ldots, N) \]

\[ t_0 = \frac{R(1 + sCR_0)}{[1 + s(C(R + R_0))]^{-1}} \]

Fig. 7. Unified SFG of N-cell interleaved converter system.

\[ t_1 < t \leq t_2, \ldots, \text{Mode-N: } t_{N-1} < t \leq t_N \]

... and generating N number of SFGs in one cycle time period for an N-cell system. This fact is in agreement with the step 8 of the proposed algorithm given in Section II.

The N SFGs \( G_1, G_2, \ldots, G_N \) are combined to form a simplified SFG and the resulting graph topology can be mathematically written as

\[ G = \sum_{j=1}^{N} K_j G_j \]  

(24)

where \( K_1, K_2, \ldots, K_N \) are the switching functions defined as

\[ K_j = \begin{cases} 
1 & \text{if } t_{j-1} < t < t_j \quad (j = 1, 2, \ldots, N) \\
0 & \text{otherwise.} 
\end{cases} \]  

(25)

While merging the SFGs \( G_1, G_2, \ldots, G_N \) into a single graph \( G \), some of the branches exist in all the graphs and some may not. Branches that exist in \( G_1 \) but not in \( G_2, G_3, \ldots, G_N \) are replaced by \( K_1 \) branches, the branches that exist in \( G_2 \) but not in \( G_1, G_3, \ldots, G_N \) are replaced by \( K_2 \) branches, and the branches that exist in \( G_3 \) but not in \( G_1, G_2, G_4, \ldots, G_N \) are replaced by \( K_3 \) branches and so on. Employing the above switching functions and the SFGs \( G_1, G_2, \ldots, G_N \), a simplified SFG is obtained as shown in Fig. 7. This is a unified SFG of an N-cell interleaved boost converter system, from which SFG of an interleaved converter system consisting of any number of cells can be obtained.

Adapting the procedure as outlined in Sections IIIA and B large-signal, steady-state and small-signal models can easily be obtained from this generalized flow graph.

A. Development of SFGs for the 2-cell Interleaved Boost Converter System

The 2-cell interleaved boost converter system is the special case of an N-cell system explained in...
the preceding section. Following the steps given in Section II B, and putting \( N = 2 \) in the \( N \)-cell converter system flow graph a unified SFG is deduced and it is shown in Fig. 8. On similar lines, as explained in Section IV for cascade boost converters, large and small-signal SFGs are drawn and they are given in Figs. 9 and 10, respectively. From these SFGs various performance characteristics can easily be obtained. However, few commonly used small-signal transfer functions and steady-state performance expressions are derived by using the well-known Mason’s gain formula [10], and they are tabulated in Tables III and IV for ready reference.
VI RESULTS AND DISCUSSIONS

Comprehensive simulation studies were made to investigate the SFG modeling of dc-dc converters. For illustration, a 2-cell cascade boost and interleaved boost converters are taken as examples to verify the theoretical analysis and SFG modeling equations developed in the preceding sections. The parameters chosen for these converters are: 1) cascade boost converter: \( L_1 = 194 \ \mu \text{H}, L_2 = 200 \ \mu \text{H}, C_1 = 200 \ \mu \text{F}, C_2 = 198 \ \mu \text{F}, \) and 2) interleaved boost converter: \( r_1 = 0.564 \ \Omega, r_2 = 0.593 \ \Omega, R_1 = 0.319 \ \Omega, L_1 = 1.2 \ \text{mH}, L_2 = 1.2 \ \text{mH}, C = 10 \ \mu \text{F}, R = 50 \ \Omega. \)

To illustrate the large-signal response analysis of the 2-cell cascade boost converter system the corresponding large-signal SFG model developed from the unified SFG (Fig. 5) was programmed in the TUTSIM simulator. Large-signal responses of the cascade boost converter were obtained for two cases: 1) supply voltage is changed from 7 to 10 V, and 2) load resistance is changed from 37 \( \Omega \) to 25 \( \Omega \) and then back to 37 \( \Omega \). For different values of the duty ratios, the step responses of the load current and voltage of the cascade converter were obtained. For illustration, few sample results are presented here for the duty ratio of 0.5 and they are shown in Figs. 11 and 12. For the duty ratio of 0.5, the 2-cell cascade boost converter system load voltage, \( V_{in} = D^{n}V_{s} \) where \( (n = 2) \), is almost four times the input voltage, which is evident from Fig. 11. In the ideal case the load voltage is almost constant against load disturbance. But in practice increase in load slightly decreases the load voltage as evidenced by the Fig. 12. To validate the SFG analysis results, experimental large-signal responses were also obtained and these results, given in the next paragraph, closely match those obtained from the SFG analysis method.
Experimental prototype circuit was bread boarded with an IGBT and fast recovery diodes (Diode: DSEI 12-06A, IGBT: IXDI30N120D1 of IXYS make). Inductor, capacitor, and load values are chosen accordingly as in simulation studies. The IGBTs are driven with international rectifier IR2110 gate driver. Experimental results are presented for the input voltage of 7 V and the duty ratio of the two IGBTs is 0.5. Converter starting response load voltage, is shown in Fig. 13. An enlarged view of the switch and load voltages is shown in Fig. 14. For the input voltage of 7 V and duty ratio of 0.5 the ideal load voltage should be around 28 V. But the experimental value obtained is about 21 V. For large-signal response studies load disturbance was created by changing the load from 37 Ω to 25 Ω and then back to 37 Ω. The results, Fig. 15, show that there is drop of about 2 V in the load voltage for a load change from 37 to 25 Ω. The discrepancy between the simulated and the experimental values is due to drops in the semiconductor devices and circuit nonidealities. This voltage drop occurs in the cascade converter, both in the first stage and second stage converters. Because of this drop the applied input voltage to the second
converter, which is the output voltage of the first converter, is less than the actual value. Hence the output voltage of second converter is affected by two factors, the reduced input voltage and drop in the second converter itself. This ultimately reduces the load voltage.

For a 2-cell interleaved boost converter, the parameter values mentioned above have been used both in simulation and prototype experimental set-up. Large-signal responses for 2-cell converter system were predicted from the SFG method for two cases: 1) supply voltage is changed from 10 to 15 V, and 2) load resistance is changed from 50 Ω to 40 Ω. These results, obtained from TUTSIM simulator, are shown in Figs. 16 and 17. To verify the SFG modeling results, experimental large-signal responses are also obtained. The corresponding results are plotted in Figs. 18 and 19. The results are closely matching and the slight discrepancies in the experimental and simulation results are mainly due to the voltage drops in the parasitics.

The above discussions show that the simulation results obtained from the SFG modeling closely match the experimental results. However, slight differences in these results are attributed to the following factors: 1) in the SFG modeling, nonidealities of the converter elements such as forward voltage drops, on-state resistances of the switching devices and other parasitics are not taken into account, and 2) errors in the measuring devices, etc.
Fig. 18. Experimental large-signal step response against supply voltage disturbance.

Fig. 19. Experimental large-signal step response against load disturbance.

VII CONCLUSIONS

General rules for drawing SPGs of dc-dc boost converters and analysis method were presented in this paper. Development of unified SFG was discussed. Large, small-signal and steady-state models for the cascade boost and interleaved boost converters lead to simple graphical circuits that are very much suitable for analysis and simulation. Analytical results, obtained from the proposed modeling method, were validated with the experimental results. Further, the performance expressions are in agreement with those obtained from state-space averaging method, thus validating the proposed modeling method.

REFERENCES

Modeling and control of DC-DC converters.

Leyva-Ramos, J. (2002)
Modeling of switch-mode dc-dc cascade converters.

Transformerless dc-to-dc converters with large conversion ratios.
Proceedings of IEEE INTELEC Conference, 1984,
455–460.
Munnadi Veerachary (M’99) was born in Survail, India, in 1968. He received the Bachelor degree from the College of Engineering, Anantapur, JNT University, Hyderabad, India, in 1992, the Master of Technology degree from the Regional Engineering College, Warangal, India, in 1994, and the Dr.Eng. degree from the University of the Ryukus, Nakagami, Okinawa, Japan, in 2002.

From 1994 to 1999, he was an assistant professor in the Department of Electrical Engineering, JNTU College of Engineering, Anantapur, India. From October 1999 to March 2002, he was a research scholar in the Department of Electrical and Electronics Engineering, University of the Ryukus, Japan. Since July 2002, he has been with the Department of Electrical Engineering, Indian Institute of Technology, New Delhi, India, where he is currently an assistant professor. His fields of interest are power electronics and applications, modeling and simulation of large power electronic systems, design of power supplies for spacecraft systems, control theory application to power electronic systems, and fuzzy neuro-controller applications to photovoltaic systems.

Dr. Veerachary was the recipient of the IEEE Industrial Electronics Society Student Travel Grant Award for the year 2001, Best Paper Award at the International Conference on Electrical Engineering (ICEE-2000) held in Kitakyushu, Japan, and Best Researcher Award for the year 2002 from the President of the University of the Ryukus, Japan. He is a member of the IEEE Industrial Electronics Society, Institute of Electrical Engineers of Japan, and Institution of Engineers India. He is listed in Who’s Who in Science and Engineering 2003.