

POWER EFFICIENT ON-CHIP OPTICAL INTERCONNECTS

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POWER EFFICIENT ON-CHIP OPTICAL INTERCONNECTS

by

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Certificate

This is to certify that the thesis titled **Power Efficient On-Chip Optical Interconnects** being submitted by **Mr. Eldhose Peter** for the award of **Doctor of Philosophy** in Department of Computer Science and Engineering is a record of bona-fide work carried out by him under my guidance and supervision at the Department of Computer Science and Engineering, Indian Institute of Technology Delhi. The work presented in this thesis has not been submitted elsewhere, either in part or full, for the award of any other degree or diploma.

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Abstract

As the number of cores on a chip increases, it gets increasingly difficult to design on-chip networks. Large networks necessitate complicated routing protocols, routers with long pipelines, and inordinate delays in transmitting messages. According to the latest ITRS report [1], optical communication will be feasible in future multi-core systems. This will ameliorate a lot of the problems in conventional networks such as high latency and low bandwidth, But, there are a lot of difficulties in implementing on-chip optical interconnects. In this work, we also concern ourselves with static power issues in optical interconnects. This issue has been regarded as the biggest bottleneck in the scalability of such networks.

We start ab initio. We begin by creating a simulation and modeling framework for basic optical components, propose some novel optical components, and later use them to create networks of varying complexities for large multicore processors.

Initially we create a set of optical components known as OptiKit. This is an open source tool kit which can be used to simulate the optical components in RSoft CAD tool. Then we create an optical network using these components. We present fast and dynamic algorithms to create an optical network in bus and tree format. These networks can support on the fly transformations. We improve this proposed network by adding a few more advanced components that can be used to make the network rearrangements quicker. After that we use this network to support fast NUCA communications by leveraging the network to send NUCA and coherence messages. Then we move on to improve the energy consumption by reducing the static power consumption. We achieve this by reconfiguring the network based on network statistics. Finally, we upgrade the network to support a huge system with 1000 nodes. This work considers the on-chip optical network in detail from the basics of optical components to a complex architecture that can support 1000s of nodes.

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